Focused Ion Beam Nanopatterning for Optoelectronic Device Fabrication

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***Abstract*—Recent photonic device structures, including distributed Bragg reflectors (DBRs), one-dimensional (1-D) or two-dimensional (2-D) photonic crystals, and surface plasmon devices, often require nanoscale lithography techniques for their device fabrication. Focused ion beam (FIB) etching has been used as a nanolithographic tool for the creation of these nanostructures. We report the use of FIB etching as a lithographic tool that enables sub-100-nm resolution. The FIB patterning of nanoscale holes on an epitaxially grown GaAs layer is characterized. To eliminate redeposition of sputtered materials during FIB patterning, we have developed a process using a dielectric mask and subsequent dry etching. This approach creates patterns with vertical and smooth sidewalls. A thin titanium layer can be deposited on the dielectric layer to avoid surface charging effects during the FIB process. This FIB nanopatterning technique can be applied to fabricate optoelectronic devices, and we show examples of 1-D gratings in optical fibers for sensing applications, photonic crystal vertical cavity lasers, and photonic crystal defect lasers.**

***Index Terms*—Focused ion beam (FIB), lithography, photonic crystal, vertical cavity surface-emitting laser (VCSEL).**

I. Introduction

FOCUSED ION BEAM (FIB) etching has been widely used as a versatile maskless lithography technique in numerous fields. FIB systems generally use an ion beam of Ga, focused to a spot size as small as 7 nm in diameter and accelerated up to 50 keV energies. Nanopatterning using FIB etching is generally employed to develop or locally modify devices, including integrated circuits [1], [2], microsystems [3], [4], and micromachining [5], [6]. Because FIB patterning saves process steps and time, it can be exploited to develop prototypes of both electrical and optical devices [7]–[11]. Direct milling on the surface [12]–[16], sputtering on a polymer layer [17]–[21], and deposition of metal using a high-energy Ga-FIB [22] can generate nanoscale patterns. Furthermore, locally modifying the GaAs surface using FIB bombardment can be applied to the selective growth of InGaAs/InP on GaAs substrate by hydride vapor phase epitaxy technique [23], [24]. Similarly, controlling the nucleation sites of Ge islands on an Si substrate using FIB patterning for quantum structure growth has been recently demonstrated [25].

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Because FIB nanolithography is generally a destructive method to generate patterns directly on the surface with small lateral dimensions, it requires a milling strategy dependent on the geometry of the pattern and inclusion of material-related issues, such as redeposition and material swelling [26], [27]. The major problems occurring during FIB patterning are sputtered material redeposition and incident ion beam contamination [28], which may alter the material properties. The sputtered material redeposition can be eliminated by using dielectric layers, and the effect of incident Ga ions is not critical in GaAs-based materials. The resolution of the defined features is fundamentally limited by the spot size of incident ion beam [29]–[31], which is typically 10 nm in diameter.

Recently, many optoelectronic devices employ subwavelength-scale structures, such as diffraction gratings, distributed Bragg reflectors (DBRs), one-dimensional (1-D) or two-dimensional (2-D) photonic crystals, and surface plasmon devices. It can be difficult to create these nanostructures using conventional photolithography. Thus, nanoscale lithography techniques such as electron beam lithography and FIB patterning are necessary. In this paper, we discuss the use of FIB as a nanolithographic tool for the fabrication of optoelectronic devices. In Section II, we first investigate the resolution of simple arrays of nanoscale holes on an epitaxially grown GaAs layer as a function of the beam current and milling time. We then present a lithographic process using a thin dielectric mask and subsequent dry etching to avoid redeposition to produce cylindrical holes. The application of this FIB nanolithography technique to fabricate novel optoelectronic devices such as optical fiber sensors, photonic crystal vertical cavity surface-emitting lasers (VCSELs), and photonic crystal defect cavities and waveguides is discussed in Section III. Section IV is a summary of our results.

II. FIB Patterning

FIB experiments are performed with an FEI Strata DB-235 Dual-beam FIB system, which is comprised of a high-resolution field emission scanning electron microscope (SEM) and a scanning Ga metal ion beam column. The 30-keV ion column with a Ga metal ion source provides ion beam current ranging from 1 pA to 40 nA. The Ga ion beam resolution is 7 nm at 1 pA beam current and a fixed 30-keV accelerating voltage. The beam spot size and resolution will vary with the ion beam current. The samples for nanohole arrays consist of epitaxially grown 100-nm-thick GaAs layer on n-GaAs substrate. Approximately 50-Å-thick film of titanium (Ti) is deposited to avoid surface charging while the samples are exposed to electron or ion beams,

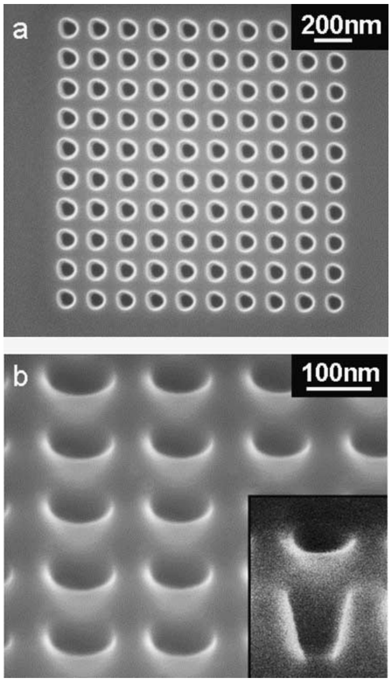

Fig. 1. (a) SEM image of 10 × 10 array holes patterned by FIB with ion beam current of 50 pA. (b) 52° perspective SEM image of the array pattern. The lower right inset shows the cross section milled by FIB. The measured depth of the hole is 125 nm.

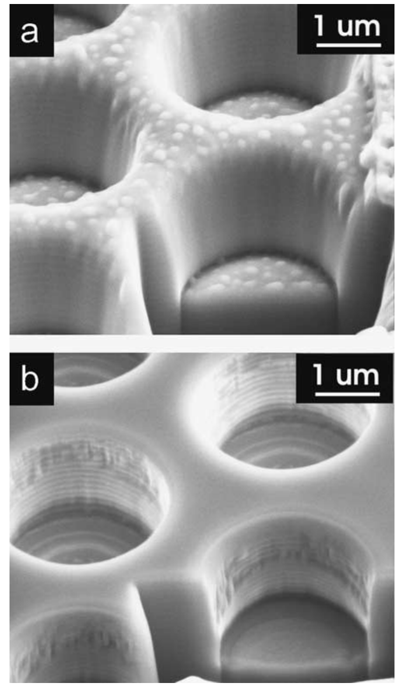

Fig. 2. (a) Holes created by FIB alone show material redeposition, surface roughness, and slightly conical shape. (b) Holes defined by FIB and etched with ICP show negligible surface roughness and are more cylindrical than holes etched with FIB alone. The lower right holes in both SEM images have been milled in cross section.

which could deform the ion beam shape. Similarly, a gold palladium alloy is typically used for Si-based materials. This Ti layer can be easily removed in a buffered oxide etch solution without damaging the GaAs materials.

Fig. 1(a) shows a 10 × 10 array of holes that are patterned using FIB with ion beam current of 50 pA and a total patterning time of 10 s. The measured period and diameter of holes are 150 and 80 nm, respectively. The designed ratio of the hole diameter to the hole period is 0.35, and thus the patterned holes in Fig. 1 are broadened by about 50%. The depth of the holes is measured to be 125 nm using an FIB milled cross section image, as shown in the inset of Fig. 1(b). The shape of the holes is affected by the aperture of the ion beam column. The diameter and depth of the hole can be controlled by changing the dwell time and beam current. For a fixed total milling time, when reducing the dwell time, the number of ion beam scans for each hole increases. Repeated scans of the ion beam into a hole result in broadening the hole. As the beam current increases, the aperture and the spot size of the ion beam increases. Thus, the size of the holes becomes larger. Therefore, a long dwell time with the smallest beam current is the best condition for patterning the smallest nanostructures using FIB. However, this also requires long milling times, and thereby we do not consider such cases in our study.

To create shallower patterns on the surface, we reduce the beam current and total milling time. Using the same pattern as in Fig. 1 with ion beam current of 1 pA and total patterning time of 7 s, the diameter and depth of the holes are measured to be 75 and 6.6 nm, respectively, using atomic force microscopy. Thus, these holes barely penetrate the 5-nm Ti layer on the GaAs layer.

In addition to the sputtered material redeposition, another drawback using FIB is the typical conical profile of the feature due to the ion beam shape and the sputtering process. Because the size of the pattern is smaller, this effect is more serious, as shown in Fig. 1. Vertical and smooth sidewalls of the hole etch profiles are desirable in many optical or electrical devices. To achieve an anisotropic hole shape, we have developed a process using FIB patterning of a thin dielectric mask layer followed by a dry etch process. This approach yields vertical sidewalls and also solves the redeposition problem. An SiO_2 or Si_3N_4 layer protects the sample surface from the redeposition and serves as the etch mask for the dry etch process. A thin Ti layer can be deposited on the dielectric layer to avoid surface charging during FIB patterning. After the FIB patterning is performed, this patterned dielectric mask is used during an inductively coupled plasma (ICP) reactive ion etch (RIE) with $SiCl_4$ as the etching gas. The ICP-RIE process is controlled to give proper hole depth and profile, and also removes the remaining Ti layer and redeposited materials on the dielectric layer. The dielectric mask layer can then be selectively removed.

Fig. 2(a) and (b) shows a comparison of the holes defined using FIB, and using the dielectric mask patterning and ICP-RIE, respectively. Redeposition of material is clearly visible in Fig. 2(a), as well as rounding of the once flat-top mirror facet between the holes. Varying the conditions of the FIB milling did not significantly alter these surface problems, although reducing the beam current with corresponding longer etching times might produce better results. Photonic crystal VCSELs [32], [33],

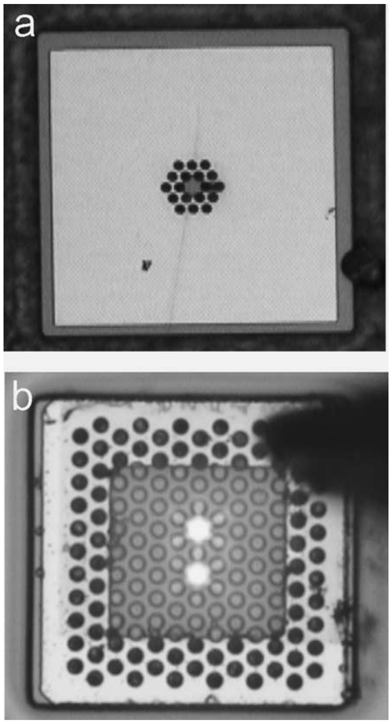

Fig. 3. (a) Photonic crystal pattern created by FIB on an implant VCSEL. (b) Multiple-defect cavity structure patterned by FIB on an oxide VCSEL. FIB enables air holes to perforate a metal contact layer.

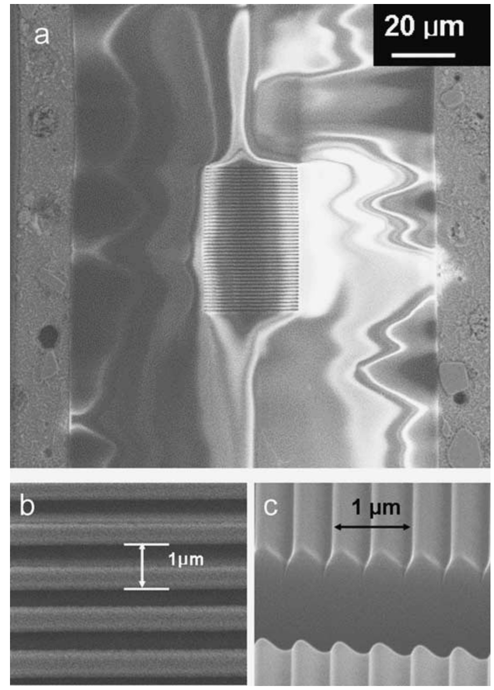

Fig. 4. (a) SEM image of 1D grating created by FIB on a side-polished optical fiber. The bright line in the center corresponds to the 5-μm fiber core. (b) SEM image of 1-μm period gratings. (c) SEM image of 500-nm period gratings and their cross section milled by FIB.

which are discussed in Section III, fabricated by FIB alone with holes as shown in Fig. 2(a) do not lase. The device shown in Fig. 2(b) is fabricated by the FIB dielectric mask patterning and subsequent ICP-RIE process. This sample has less surface damage and redeposition. We observe that etched holes retain their cylindrical shape in deeper etches as compared with direct FIB etching cases, where the holes take on a more conical appearance.

Electron beam (EB) lithography has been also used to define nanoscale patterns. Both EB lithography and FIB patterning can create nanoscale patterns, but each method has performance advantages and inherent limitations. The EB lithography process is done using an EB resist such as polymethylmethacrylate, which transfers a pattern to another mask material. FIB can directly generate mask patterns into a dielectric layer without a resist. Thus, the FIB patterning process has an advantage for development of prototype devices. Unlike EB lithography, FIB can define patterns on the sample with height variations such as a mesa and a ridge because it does not need to spin coat a resist. FIB can also achieve grayscale patterns by controlling the beam current and milling time, whereas EB lithography is a binary process. In addition, FIB enables patterns to perforate a metal layer. As shown in Fig. 3, air holes on a fabricated VCSEL sample are created through 2000-Å-thick Ti/Au metal contact layer. This is a unique capability of FIB patterning. Furthermore, this technique can also be used to create a periodic pattern or a single hole in the metal layer for studying surface plasmonics [34].

III. Optoelectronic Applications

A. *Optical Fiber Gratings*

Many applications of side-polished optical fibers, including temperature and pressure sensors, communication components such as filters [35], switches [36], and polarizers [37], have been reported since the late 1970s. Side-polished fibers are obtained by polishing nearly half the optical fiber to access the evanescent field from the fiber core. The evanescent field exponentially decays with the distance from the interface between the core and cladding. The interaction between the evanescent field and a deposited waveguide, a metallic layer, or a grating on the side-polished region modifies wavelength, polarization, or output power. The change of an optical signal in the fiber can be used to sense environmental changes such as pressure [38] and temperature [38]–[40]. We employ the FIB patterning technique to create a 1-D fiber Bragg grating on the side-polished fiber. Fig. 4 shows 1-μm and 500-nm period gratings on the side-polished fiber. In Fig. 4(a), charging by nonconducting materials in the optical fiber causes the fringes around the grating pattern. The bright line in the center corresponds to the 5-μm fiber core. The 1-D fiber gratings in Fig. 4(a) and (b) is patterned using FIB with an ion beam current of 1000 pA and a dwell time of 1000 μs on the area of 30 $\times$ 40 μm. Although the direction of FIB milling is programmed to move vertically, the generated horizontal gratings are fairly uniform over the entire pattern. Fig. 4(c) shows 500-nm period gratings and their FIB milled cross section. In this case, because the FIB milling is performed along the direction of the grating, the grating is sharper and straighter than in Fig. 4(b).

B. Photonic Crystal VCSEL

Two-dimensional photonic crystal structures etched into the top mirror of a VCSEL have been investigated as a means of achieving lateral mode control [32], [33]. The method we use for fabricating such a structure on a prefabricated VCSEL employs FIB patterning. This procedure may enable custom transverse mode engineering in commercial VCSEL manufacturing. FIB etching has previously been applied to VCSEL fabrication, primarily for modal control. Introducing mirror loss around a central region can give rise to a single-mode device [41], and polarization control can be achieved using targeted milling [42], and grayscale milling [43].

FIB etching is suitable as a postprocessing method for adding a photonic crystal pattern of holes to an existing VCSEL. FIB etching permits the photonic crystal pattern to be etched into a VCSEL facet without the need to first define the pattern through a mask. This allows the exploitation of the unique benefits of the photonic crystal structure without significantly altering the VCSEL. EB lithography [33] and optical lithography [32] have both been used successfully to pattern the photonic crystal design, but are not suitable as a postprocessing technique because of the need to spin coat resist. The process described in the following can be used after conventional VCSEL fabrication on one or many specifically selected VCSELs within a wafer, die, or packaged component.

A triangular pattern consisting of 2.8-μm diameter photonic crystal holes with a lattice spacing of 4 μm is etched into a prefabricated oxide-confined VCSEL with a 32 $\times$ 32 μm square oxide aperture, as shown in Fig. 5(a). The prefabricated VCSELs contain 25 pairs in the top DBR. As discussed in Section II, an etch mask layer of silicon dioxide is deposited on the surface of the prefabricated VCSEL, and the FIB with an ion beam current of 5000 pA is used to define a photonic crystal pattern on this etch mask layer. The FIB can remove the SiO_2 mask layer and any underlying metal contact layer to define the pattern (Fig. 3). This patterned silicon dioxide mask is used during an ICP-RIE with $SiCl_4$ as the etching gas. Finally, the remaining SiO_2 mask layer is then selectively removed. Fig. 5(a) and (b) shows the near-field pattern and spectrum, respectively. A side-mode suppression ratio of more than 30 dB is achieved, showing the utility of the photonic crystal in the VCSEL. We have also used this process to successfully fabricate other photonic crystal designs, such as 7-point defect structures [33], and multiple defect cavity structures [44].

C. Photonic Crystal Defect Lasers

There has been increasing interest in photonic crystal defect lasers [45], [46] because they are candidates for the next generation nanophotonic light sources. Photonic crystal lasers are 2-D photonic crystal slab structures based on periodic air holes perforated through about one half wavelength thick membrane waveguide, as shown in Fig. 6. In this structure, the 2-D photonic crystal pattern provides in-plane confinement, and the air-suspended semiconductor slab permits total internal reflection of the light in the vertical direction. The optical cavity is created by a defect, which is one or more missing air holes [47], and

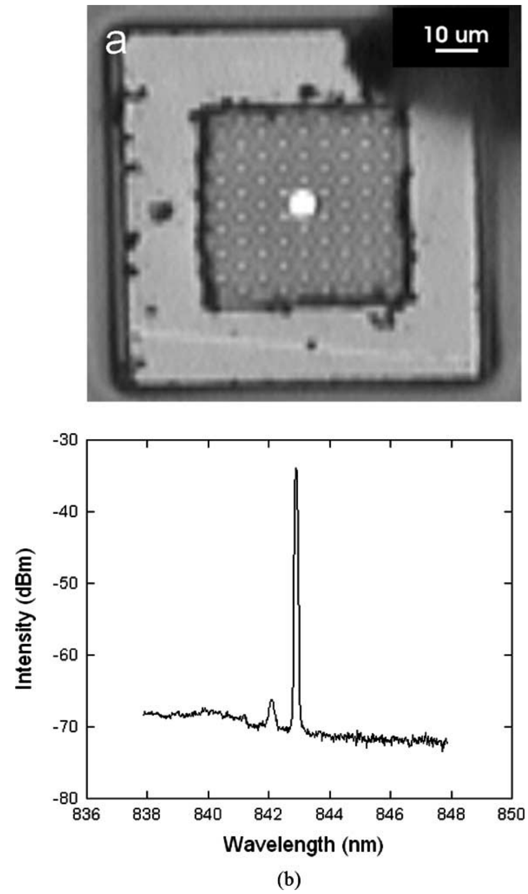

Fig. 5. (a) Near-field pattern of a photonic crystal defect lasing in the fundamental mode. (b) Spectrum of the photonic crystal VCSEL.

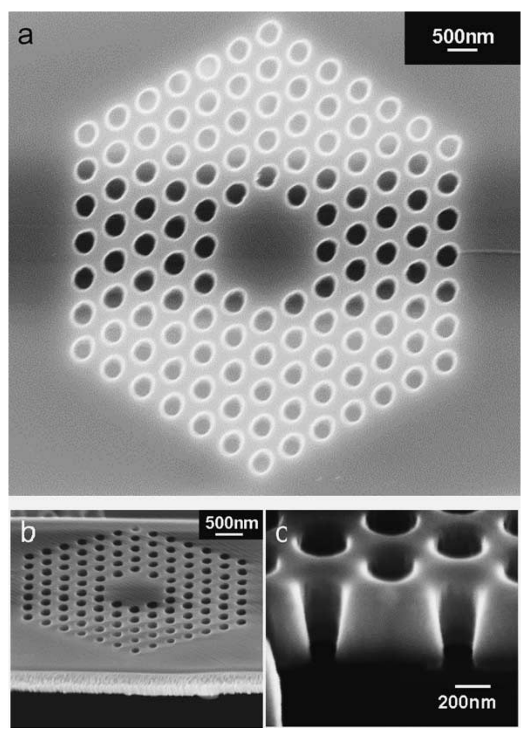

Fig. 6. (a) SEM image of a photonic crystal defect cavity structure defined by FIB. (b) 60° perspective SEM image of an undercut etched sample. (c) FIB milled cross section SEM image of an undercut etched sample.

thus the optical modes can be strongly localized in this defect region. The manipulation of the local refractive index around the defect can determine the cavity optical properties, such as the wavelength and polarization of the 2-D photonic crystal laser. The local index modification arising from the photonic crystal can be achieved by lithographic control of the defect size, shape, or position [48].

When the cavity designs (including lattice spacing, diameter of holes, and lattice pattern) are determined from the photonic band structure, the photonic crystal patterns must be transferred into the materials. The sample shown in Fig. 6 consists of 400-nm GaAs and 600-nm AlAs layers epitaxially grown on the GaAs substrate. A thin dielectric layer (~1000 Å SiO_2) is deposited by plasma-enhanced chemical vapor deposition for the etch mask with 50-Å-thick Ti layer on top. FIB milling is performed at 100- and 300-pA beam current with 30-keV Ga ion beam. The photonic crystal pattern can be directly transferred to Ti/SiO_2 mask under the precise control of FIB. Then, ICP-RIE with $SiCl_4$/Ar plasma perforates the air holes into the semiconductor slab using the FIB patterned Ti/SiO_2 mask. During the ICP-RIE process, most of the Ti layer is also etched away. The remaining Ti/SiO_2 layer can be easily removed by following a diluted hydrofluoric acid etching to remove the 600-nm AlAs sacrificial layer under the GaAs slab. Fig. 6(b) and (c) shows an undercut etched photonic crystal structure. The lattice spacing and diameter of holes are 350 and 200 nm, respectively. Because the sidewall of the FIB milled pattern in the Ti/SiO_2 layer is not very cylindrical, the measured r/a ratio of the actual pattern in the slab is smaller than that desired (~250 nm). The FIB lithographic pattern relies sensitively on the conditions of the ion beam column, so reproducibility and uniformity are not as good as those of EB lithography. Furthermore, the field of view in SEM of the FIB limits the pattern area. It is difficult to create more than about ten photonic crystal periods in a single pattern.

IV. Conclusion

We describe the use of FIB milling for nanolithographic patterning of optoelectronic devices. We briefly study the advantages of FIB, and then describe the FIB nanopatterning technique for creating air holes on an epitaxially grown GaAs layer and 1-D gratings on a side-polished optical fiber. We present a postprocessing method using a dielectric (SiO_2) mask and subsequent dry etching for introducing photonic crystal patterns into VCSELs to control their modal properties. By using a dielectric layer that is patterned by FIB, we avoid using resists and redeposition of material. We can also gain benefit from the versatility of the postfabrication process. This approach can also be used to fabricate photonic crystal defect laser structures. Thus, the FIB patterning process described is a useful nanoscale lithographic tool.

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