Etch damage and deposition repair of vertical-cavity surface-emitting lasers

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Dielectric layers are often employed as etch masks for mesa and trench structures during vertical-cavity surface-emitting laser (VCSEL) fabrication. The removal of these mask layers by reactive ion etching results in unavoidable exposure of the top laser facet to sputtering. This sputtering is experimentally shown to impact the device performance. After a thickness of less than a quarter wavelength (~60 nm) has been removed, the VCSELs are no longer able to achieve lasing threshold. Simulation indicates that the reason for this is a decrease in quality factor by more than an order of magnitude. Consistent with this explanation is that the damage can be partially repaired (allowing laser oscillation) by depositing SiO_2 to compensate for the missing semiconductor material. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2150222]

I. INTRODUCTION

In recent years, vertical-cavity surface-emitting lasers (VCSELs) have become commercially viable for use in short-haul optical data communication applications which require low-power operation and high-volume, low-cost manufacture, resulting in VCSELs with excellent reliability. During VCSEL fabrication, the deposition and removal of dielectric layers are often employed. For example, to fabricate oxide-confined VCSELs, mesas or trenches are etched to expose the layers to be converted to Al_2O_3.[1] Because anisotropy which results from wet etching is undesirable, reactive ion etching (RIE) is most often used. Dielectric layers composed of SiO_2 or SiN_x are usually used as the etch mask for the Cl-based RIE and subsequently are removed using a freon (CF_4 or CHF_3) RIE process. Uncertainties in the mask selectivity during the Cl-based etch and variations in the freon RIE etch rate during the mask removal result in the top facet of the VCSEL being exposed to the freon etch for some length of time.

Ion-induced damage to GaAs during RIE)[2] and ion milling[3,4] has been previously characterized. In this work, the physical damage caused to the top of the VCSEL by the RIE exposure is found to adversely affect mirror reflectivity, scattering loss, absorption loss, and phase mismatch, all of which affect laser performance. Following the etch damage, we show that SiO_2 deposited by plasma-enhanced chemical-vapor deposition (PECVD) can replace the material which is removed by the RIE and restore lasing operation. Limitations which prevent a full repair of the damaged devices are also discussed.

II. EXPERIMENT

The VCSEL device structure for this experiment consists of a bottom *n*-type 36-period distributed Bragg reflector (DBR), an undoped active region with five GaAs quantum wells, and a top *p*-type 21-period DBR, all of which were grown by metal-organic vapor-phase epitaxy and designed for a wavelength of 850 nm.[1] Repeating layers of $Al_{0.16}Ga_{0.84}As/Al_{0.92}Ga_{0.08}As$ form the DBRs and one $Al_{0.98}Ga_{0.02}As$ layer was grown on each side of the active region for selective oxidation.[5–7] A backside contact (AuGe/Ni/Au) was deposited to form an ohmic contact to the *n*-type substrate, and top ring contacts (Ti/Au) were lithographically patterned and formed by lift-off after the metal deposition. The mesa structure was created by $SiCl_4/Ar$ inductively coupled plasma reactive ion etching using SiO_2 as the etch mask. The high-Al layers were oxidized to provide electrical and optical confinements, and the etch mask was removed using the optimal CF_4 RIE process which is discussed next. A cross-sectional schematic of a fabricated VCSEL is shown in Fig. 1.

Optimization of the CF_4 RIE etch process to provide maximum selectivity of etched SiO_2 to sputtered GaAs was done as follows. GaAs test samples were prepared by depositing 400 nm of SiO_2 by SiH_4/N_2O PECVD in a conventional commercial reactor, with a deposition rate of 11.5 nm/min.[8] Samples of photoresist-patterned GaAs and SiO_2-coated GaAs were etched in the RIE reactor under various plasma conditions and various times. The rf power was varied between 27 and 190 W and pressure was varied between 15 and 100 mT. Following each etch, the photoresist was removed and the etch rate for SiO_2 and sputter rate for GaAs were determined. The optimal process giving the highest etch selectivity of SiO_2:GaAs and the best repeatability was found to etch SiO_2 at about 25 nm/min and sputter GaAs at 4 nm/min for an overall SiO_2:GaAs selectivity better than 6:1.

Using the optimized dielectric RIE process, the VCSELs were subjected to this etch and subsequently characterized. The characterization included the continuous wave (cw) light versus current (LI) measurements at room temperature, and the top facets of the VCSELs were examined using scanning electron microscopy (SEM) and an atomic force microscopy

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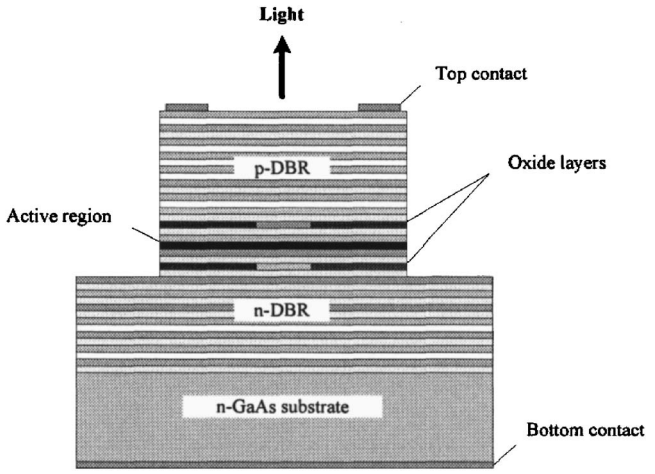

FIG. 1. Cross-sectional schematic of the VCSEL structure.

(AFM) system using a Si_3N_4 tip running in tapping mode. The VCSELs were exposed in 2 min increments to the CF_4 RIE process and then characterized. This procedure was repeated until the VCSELs stopped lasing.

In an effort to repair the damage caused to the top facet, SiO_2 was deposited by PECVD. These depositions also took place in 2 min increments (~20 nm per iteration), with LI measurements done between each deposition. The index of refraction of SiO_2 deposited by PECVD is approximately 1.5, compared with the top facet layers of the VCSEL device structure (GaAs cap layer plus $Al_{0.16}Ga_{0.84}As$) which have an index of refraction of approximately 3.5. Once the appropriate thickness was achieved and the laser operation was confirmed, AFM and SEM images were reacquired.

III. RESULTS AND ANALYSIS

Figure 2 illustrates the LI characteristics of a 5×5 μm^2 aperture VCSEL at various stages during the RIE etch process. This plot shows an increase in threshold current as the top DBR facet is etched away. After an initial increase, the maximum power and slope efficiency are also reduced, and after 48 nm of material is removed from the top facet, the device can no longer achieve lasing threshold. Figure 3(a) plots the differential quantum efficiency as a function of the RIE etch depth of the top DBR; this distance is also normalized to the wavelength in the material for easy comparison. The differential quantum efficiency is the ratio of output photons to the input carriers and can be measured from the slope efficiencies of the LI curves in Fig. 2. The general trend of the graph shows increasing quantum efficiency as the material is sputtered away until a critical point is reached where catastrophic degradation in performance occurs.

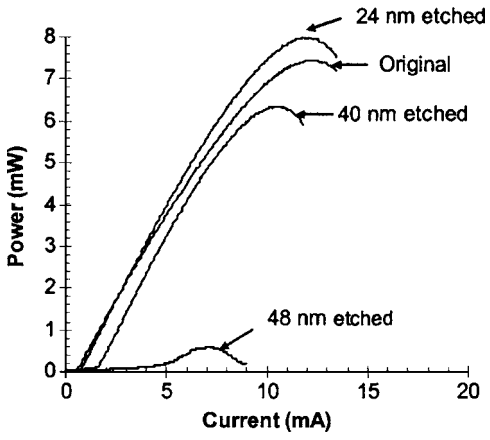

FIG. 2. LI characteristics at various DBR etch depths.

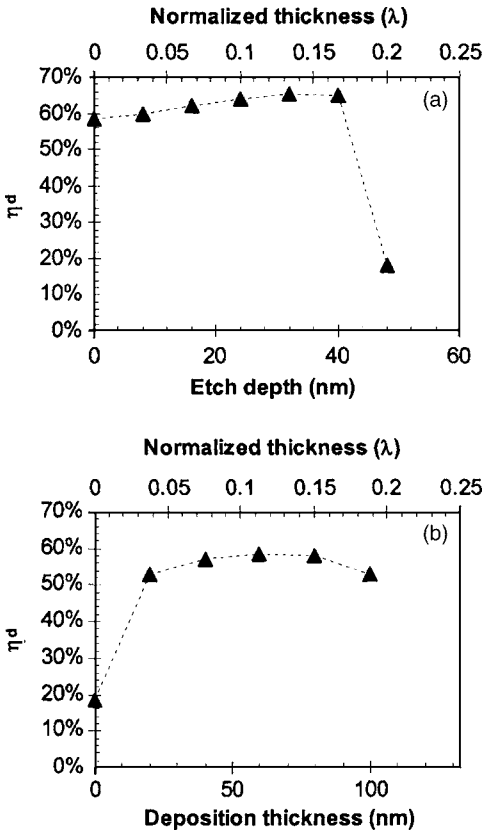

FIG. 3. Differential quantum efficiency as a function of RIE etch depth (a) and PECVD SiO_2 deposition thickness (b).

To explain these results, a general understanding of VCSEL operation is required.[1] Laser oscillation requires two general conditions: the round-trip modal gain must equal the round-trip modal loss and the cavity must be resonant. The cavity quality factor Q is a numerical measure of the cavity resonance, taking into account all cavity losses. A larger Q indicates stronger resonance and less losses, which can be translated to lower laser threshold current. Because they cannot achieve arbitrarily large gain, VCSELs typically require Q values greater than a few thousand for laser operation to occur.

In the first part of the experiment, sputtering of the top DBR facet led to an initial increase in differential quantum efficiency η_d which is given by

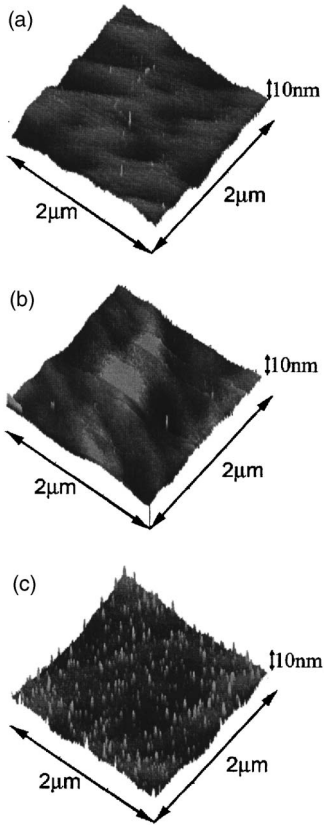

FIG. 4. AFM images of the top DBR surface taken before RIE (a), after RIE (b), and after SiO_2 deposition (c).

$$\eta_d = \left(\frac{h\upsilon}{q}\right)\frac{\alpha_m}{\alpha_m + \alpha_{\text{abs}} + \alpha_{\text{scat}}}, \tag{1}$$

where h is Planck's constant, υ is the frequency of oscillation, q is the electron charge, α_{abs} is the loss due to absorption, α_{scat} is the loss due to optical scattering, and α_m is the output mirror loss. AFM scans of the DBR surface before and after exposure to the RIE are shown in Figs. 4(a) and 4(b), respectively. As shown, the surface topography does not noticeably change as a result of the etch, suggesting that α_{scat} remains relatively constant. The increase in η_d is therefore attributed to both an increase in α_m and a decrease in α_{abs}. DBR reflectivity calculations following[1] predict an increase in the mirror loss as the top surface is etched, effectively detuning the phase matching at the top facet. The reduction of absorption loss is caused by the removal of the thin GaAs cap layer (which exhibits high band-edge absorption) and a significant amount of the top highly-doped AlGaAs current-spreading layer (which contributes to free-carrier absorption).

The differential quantum efficiency peaks after approximately 32 nm ($\lambda/8$) of the top DBR has been etched away. Further etching causes a rapid decrease in η_d. To help explain this, the lossless transmission through the entire VCSEL structure was simulated[1] and Q was calculated using

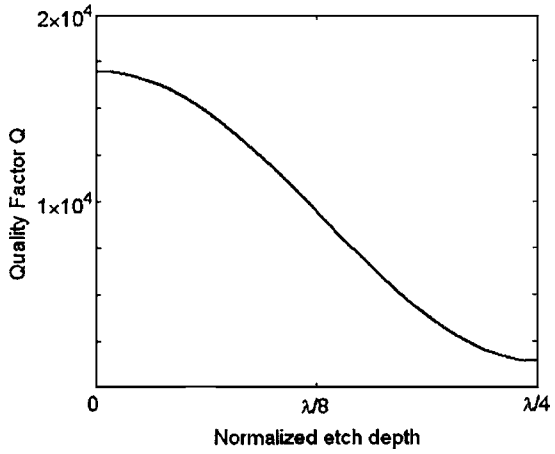

FIG. 5. VCSEL cavity quality factor Q vs normalized etch depth.

$$Q = \frac{\lambda_0}{\Delta\lambda_{1/2}}, \tag{2}$$

where λ_0 is the peak resonance frequency of the cavity and $\Delta\lambda_{1/2}$ is the full width at half maximum of the cavity resonance spectrum. The Q factor versus normalized etching depth is shown in Fig. 5. An order-of-magnitude decrease in Q occurs by the sputtering of only 60 nm ($\lambda/4$) from the top facet. Initially, as Q is decreased, more light can couple out of the VCSEL, increasing the power and differential quantum efficiency (at a cost of higher threshold). However, as Q is further decreased, saturation and thermal effects prevent the VCSEL from reaching high enough optical gain for laser action to occur. As evident in Fig. 2, we estimated that 48 nm was sputtered away from the nonfunctioning VCSEL. This explanation is consistent with the initial increase in maximum output power and efficiency followed by the catastrophic degradation which was shown in Fig. 2.

Figure 6 illustrates the LI characteristics as the top DBR is coated by SiO_2 layers. The original LI characteristics from the undamaged device are also plotted for comparison. The added material increases the optical path length, causing Q to

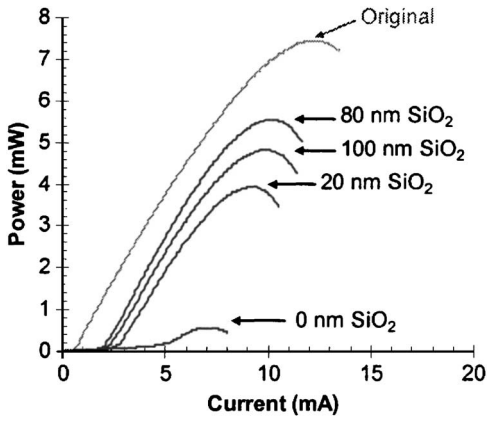

FIG. 6. LI characteristics at various stages of SiO_2 deposition repair. The original undamaged device LI curve is plotted for reference. Note that maximum performance was achieved for 80 nm deposited SiO_2.

increase and laser operation is restored. The differential quantum efficiency as a function of deposited SiO_2 thickness is shown in Fig. 3(b). From these figures it is clear that the device never fully recovers from the RIE sputter damage; there are two possible reasons for this. First, as shown in Fig. 4(c), the surface profile was roughened as a result of the SiO_2 deposition. Small islands formed on the surface during the deposition process can cause an increase in α_{scat}. Second, because the highly-doped current-spreading layer was removed in the first part of the experiment, the repaired device no longer laterally distributes the current as well as the original. The resulting nonuniform current profile requires higher total current to achieve the same constant current density across the lasing aperture.

IV. CONCLUSIONS

This work investigates the detrimental effect of exposure of the top facet of a VCSEL to a CF_4 RIE, which is often used to remove dielectric layers from VCSELs. Completely avoiding this exposure is an obvious solution to this problem, but even slight exposure of the bare facet is shown to alter the lasing properties. Although chemical etching of the top surface does not occur, the kinetic sputtering of the surface leading to material removal can greatly alter the cavity quality factor. This damage is at least partially reversed by depositing a dielectric layer to reestablish proper phase matching at the top facet. The degree to which the devices could be repaired is dependent both on the uniformity of the deposited dielectric and the reduction in current-spreading capability. Accounting for facet damage during fabrication should improve VCSEL manufacturing yield, enable higher performance, and potentially improve reliability.

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