

# Optical AND/OR gates based on monolithically integrated vertical cavity laser with depleted optical thyristor structure

Woon-Kyung Choi, Doo-Gun Kim, Do-Gyun Kim, and Young-Wan Choi

Microwave and Lightwave Telecommunications Lab., School of Electrical and Electronic Engineering,  
Chung-Ang University, 221 Heuksuk-Dong, Dongjak-ku, Seoul, 156-756, Korea

[ychoi@cau.ac.kr](mailto:ychoi@cau.ac.kr)

<http://mlt.cau.ac.kr>

Kent D. Choquette

Electrical and Computer Engineering Dept., University of Illinois at Urbana-Champaign,  
208 N. Wright Street, Urbana, IL, 61801, USA

Seok Lee and Deok-Ha Woo

Photonics Research Center, Korea Institute of Science and Technology, 39-1 Hawolgok,  
Seongbuk, Seoul 136-791, Republic of Korea

**Abstract:** Latching optical switches and optical logic gates with AND and OR functionality are demonstrated for the first time by the monolithic integration of a vertical cavity lasers with depleted optical thyristor structure. The thyristors have a low threshold current of 0.65 mA and a high on/off contrast ratio of more than 50 dB. By simply changing a reference switching voltage, this single device operates as two logic functions, optical logic AND and OR. The thyristor laser fabricated by using the oxidation process and has achieved high optical output power efficiency and a high sensitivity to the optical input light.

©2006 Optical Society of America

OCIS codes: (250.7260) Vertical cavity surface emitting lasers; (130.3750) Logic devices; (200.4660) Optical logic

---

## References and links

1. P. Zhou, J. Cheng, C. F. Schaus, S. Z. Sun, C. Hains, D. R. Myers, and G. A. Vawter, "Versatile bistable optical switches and latching optical logic using integrated photothyristors and surface-emitting lasers," *Dig. 1991 Int. Electron Device Meet. Washington, DC*, **1**, 611-614 (1991).
2. K. Kasahara, Y. Tashiro, N. Hamao, M. Sugimoto, and T. Yanase, "Double heterostructure optoelectronic switch as a dynamic memory with low-power consumption," *Appl. Phys. Lett.* **52**, 679-681 (1988).
3. H. Martinsson, J. A. Vukusic, M. Grabberr, R. Michalzik, R. Jager, K. J. Ebeling, A. Larsson, "Transverse mode selection in large-area oxide-confined vertical-cavity surface-emitting lasers using a shallow surface relief," *IEEE Photon. Technol. Lett.* **11**, 1536-1538 (1999).
4. S. Kawai, K. Kasahara, and K. Kubota, "Vstep Optoelectronic Devices and Their Modules," *LEOS 1992 Summer Topical Meeting* **1**, C28-C29 (1992).
5. G. R. Olbright, R. P. Bryan, K. Lear, T. M. Brennan, G. Poirier, Y. H. Lee, and J. L. Jewell, "Cascadable laser logic devices: discrete integration of phototransistors with surface-emitting laser diodes," *Electron. Lett.* **27**, 216-217 (1991).
6. I. Ogura, H. Kosaka, T. Numai, M. Sugimoto, and K. Kasahara, "Cascadable optical switching characteristics in vertical-to-surface transmission electrophotonic devices operated as vertical cavity lasers," *Appl. Phys. Lett.* **60**, 799-801 (1992).
7. C. W. Wilmsen, F. R. Beyette, Jr., X. An, S. A. Feld, and K. M. Geib, "Smart pixels using the light amplifying optical switch (LAOS)," *IEEE J. Quantum Electron.* **29**, 769-774 (1993).
8. P. Zhou, J. Cheng, C. F. Schaus, S. Z. Sun, C. Hains, K. Zheng, E. Armour, W. Hsin, D. R. Myers, and G. A. Vawter, "Cascadable, latching photonic switch with high optical gain by the monolithic integration of a vertical-cavity surface-emitting laser and a pn-pn photothyristor," *IEEE Photon. Technol. Lett.* **3**, 1009-1011 (1991).

9. W. K. Choi, D. G. Kim, Y. W. Choi, K. D. Choquette, Y. K. Kim, S. Lee, and D. H. Woo, "Optical properties of selectively oxidized vertical cavity laser with depleted optical thyristor structure," *Appl. Phys. Lett.* **89**, 121117 (2006).
10. W. K. Choi, D. G. Kim, Y. W. Choi, S. Lee, D. H. Woo, and S. H. Kim, "AlGaAs/GaAs NpnP depleted optical thyristor using bottom mirror layers," *Jpn. J. Appl. Phys.* **44**, 2913-2920 (2005).
11. C. Wilmsen, H. Temkin, and L. Coldren, *Vertical Cavity Surface Emitting Lasers* (Cambridge Univ. Press, 1999), Chap. 5.
12. K. D. Choquette, R. P. Schneider Jr., K. L. Lear and K. M. Geib, "Low threshold voltage vertical-cavity lasers fabricated by selective oxidation," *Electron. Lett.* **30**, 2043-2044 (1994).
13. B. Lu, P. Zhou, Y. Lu, J. Cheng, R. E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S. A. Chalmers, and G. A. Vawter, "Binary optical switch and programmable optical logic gate based on the integration of GaAs/AlGaAs surface-emitting lasers and heterojunction phototransistors," *IEEE Photon. Technol. Lett.* **6**, 398-401 (1994).
14. P. Zhou, J. Cheng, C. F. Schaus, S. Z Sun, C. Hains, E. Armour, D. R. Myers, and G. A. Vawter, "Inverting and latching optical logic gates based on the integration of vertical-cavity surface-emitting lasers and photothyristors," *IEEE Photon. Technol. Lett.* **4**, 157-159 (1992).

## 1. Introduction

Vertical cavity surface emitting laser based optical switches and optical logic gates provide a versatile and promising approach to two-dimensional optical information processing, parallel computing, and interconnection architectures because of their monolithic integrability, surface-normal format, functional flexibility [1,2], parallel optical access, low beam divergence [3], and good modal properties [4-6]. Optical switches and logic gates provide the building blocks for these optical networks, while latchable optical gates and flip flops are the essential elements for optical memories. Latching optical logic gates also have the advantages of lower switching energies, higher optical gain, and a larger input signal dynamic range [7, 8]. All the Boolean logic functions can be constructed by using only two basic logic functions, such as AND or OR, plus the INVERT function. Any logic function can be implemented by cascading different combinations of these simple gates. However, cascading logic gate arrays entails significant bulk optical components and optical packaging. To perform complicated integrated logic functions, it is always desirable to minimize the component count and thus simplify the interconnections and thermal management problems. This is particularly important in the monolithic integration of a multifunctional logic chip where cascading may not be possible. This paper demonstrates that a monolithically integrated vertical cavity laser with depleted optical thyristor (VCL-DOT) structure can be configured into many optical logic functions using a simple operating technique which is changing the condition of the driving voltage.

## 2. Basic operations

An optical thyristor is a bistable device with an s-shaped current-voltage (I-V) characteristic as shown in Fig. 1. Here, the switching voltages ( $V_{S1}$ ,  $V_{S2}$ ,  $V_{S3}$ ) are the forward breakdown voltages, and  $I_S$  is the switching current. In the forward bias, the thyristor has three distinct states: (1) high-impedance forward blocking region (off-state), (2) negative-resistance region, and (3) low-impedance and high-conductance forward-conducting region (on-state). In the on-state, the optical thyristor emits light as a laser. By increasing the input optical power, it is possible to vary the I-V curve from  $C_1$  to  $C_3$ . Load lines  $L_1$  and  $L_2$  are obtained with proper external circuits. Two stable operating points  $S_1$  and  $H_1$  are obtained with the load-line  $L_1$  indicating off- and on-state, respectively.

The double-heterostructure optical thyristor (DHOT) is shown in Fig. 2(a) with an external resistor ( $R$ ) and a driving voltage ( $V_D$ ).  $S$  is an optical input and  $Q$  is an optical output of the thyristor. As shown, there are three pn junctions  $J_1$ ,  $J_2$  and  $J_3$  in a DHOT. Figure 2(b) shows the timing diagram of the optical signal ( $S$ ) and the external driving voltage necessary for switching and the optical output signal ( $Q$ ). Though  $V_D$  is lower than switching voltage ( $V_S$ ), the thyristor should be in the on-state when the incident optical signal is injected into the thyristor. Because the carriers are generated in the gate layers under the incident light beam, the switching voltage is reduced. These characteristics are required in order for the optical thyristor to be switched. This method is proper for operating a single device. The state of a

DHOT can be read out optically because the optical thyristor emits an optical signal only in the on-state [10].

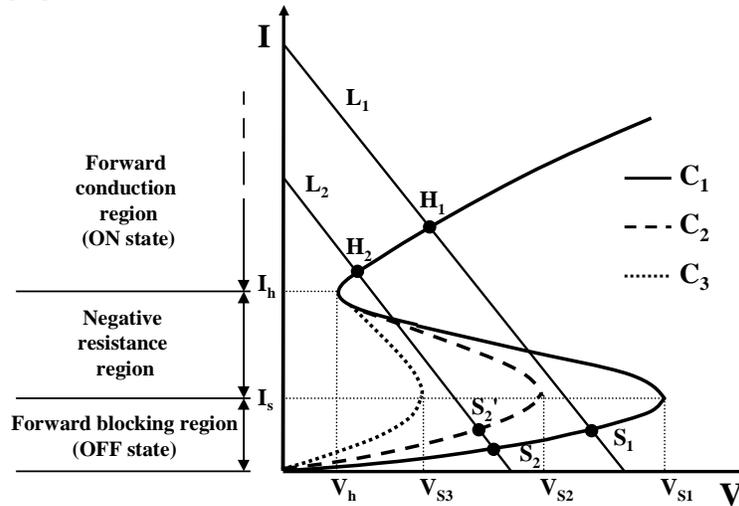


Fig. 1. Typical S-shaped current-voltage characteristic of an optical thyristor.

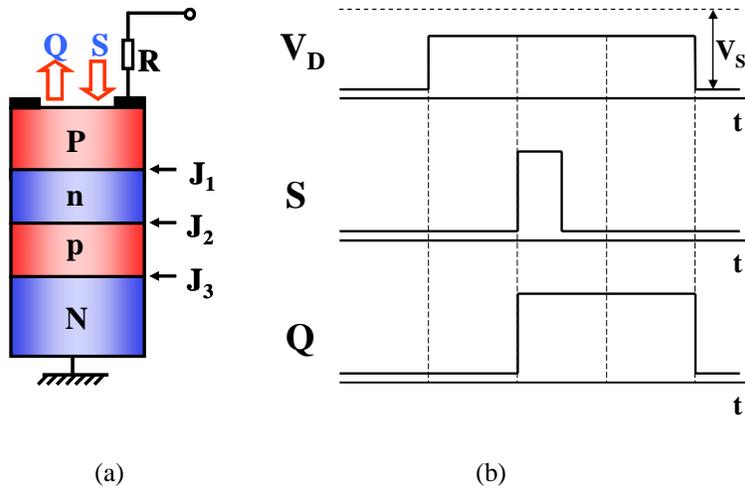


Fig. 2. (a). Cross-section of optical thyristor structure with external resistor (R) and driving voltage ( $V_D$ ). (b). optical pulse and voltage pulse for single operation.

Now let's assume that the two optical input signals are injected into the thyristor.  $C_1$  is the original I-V curve,  $C_3$  is the I-V curve when two optical input signals are injected, and  $C_2$  is the I-V curve when only one is injected into the thyristor. When the driving voltage between  $V_{S2}$  and  $V_{S3}$  is applied to the optical thyristor, as shown in the load line  $L_2$ , it should turn-on at only the  $C_3$  condition because the operating points ( $S_2$  and  $S_2'$ ) are in the off-state at  $C_1$  and  $C_2$  conditions and it is able to move to  $H_1$  in the on-state from the only  $C_3$  condition, thus providing a logical AND function. However, when the driving voltage is changed to the value between  $V_{S1}$  and  $V_{S2}$  like  $L_1$ , it should turn-on at  $C_2$  and  $C_3$  conditions, thus providing a

logical OR operation. In other words, this operating technique allows the optical thyristor to achieve both of the logical AND- and OR-gates by very simple adjustment of the load line. This is very suitable for integrating an optical thyristor with electronic devices for optoelectronic integrated circuits and various applications such as optical logic systems.

### 3. Results and discussions

VCL-DOT structure is grown by metal organic chemical vapor deposition. The PnpN active region is surrounded by two distributed Bragg reflectors with continuously graded transition layers, which significantly reduced the threshold voltage and series resistance of the laser. Details of the structure, the processing steps, and the electrical and optical properties are described in previous work [9].

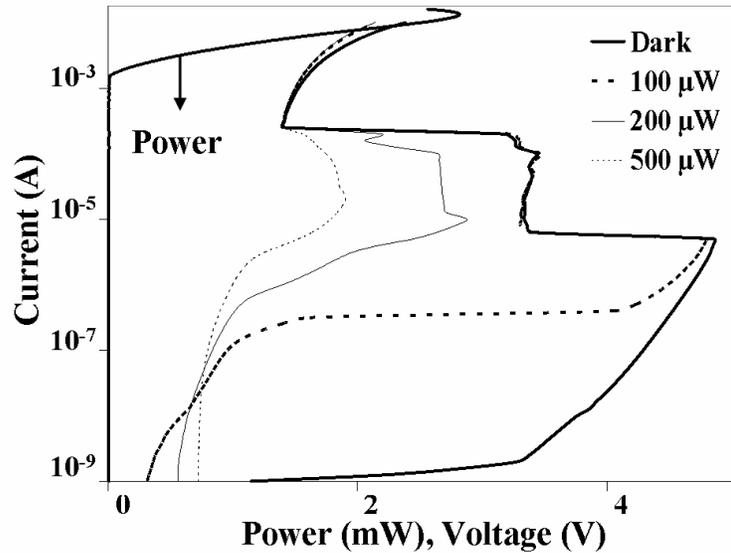
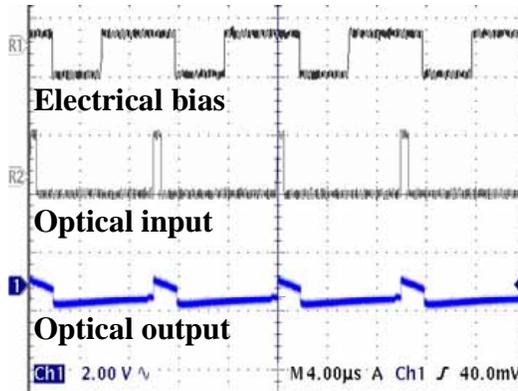
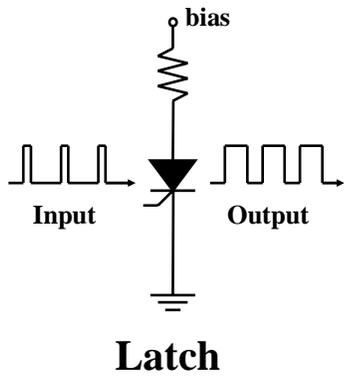
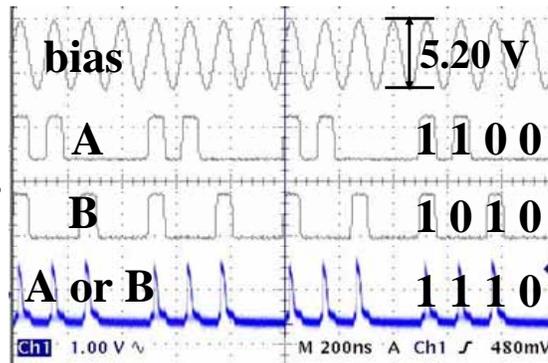
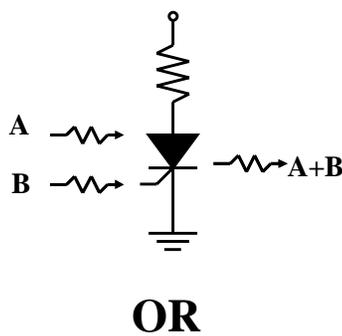


Fig. 3. Current-voltage-light characteristics of the integrated VCL-DOT, showing changes of bistable electrical characteristics by optical input light intensity.

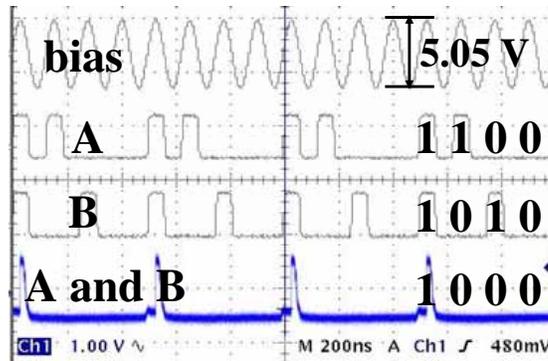
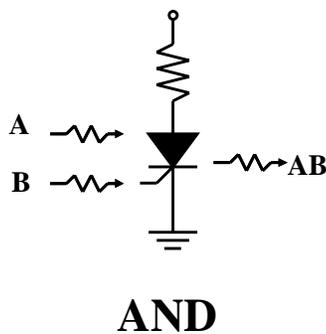
Figure 3 is the room temperature, continuous wave, log plot of the light(L)-current(I)-voltage(V) characteristics of the integrated VCL-DOT with an oxide aperture of  $5 \times 5 \mu\text{m}$  as a function of input light intensity causing a switching transition. For forward bias, the optical thyristor experimentally shows the nonlinear s-shaped I-V characteristic with three distinct states: the low-current OFF-state, the high-current ON-state, and the negative resistance region. In the OFF-state, The I-V curve exhibits a bistable electrical behavior, with switching and holding voltage 5.24 and 1.50 V, and switching and holding currents of  $5 \mu\text{A}$  and  $100 \mu\text{A}$ , respectively. The switching voltages are clearly decreased from 5.24 V to 1.90 V as the external optical input intensity changes from zero to  $500 \mu\text{W}$ . The threshold current of the VCL-DOT is 0.65 mA, and its output power is 2.17 mW at a drive current of 8 mA. This threshold current is very low due to a reduction of current spreading and elimination a leakage current through the side walls. The device reported here can achieve high sensitivity without any additional passivation processing [11, 12]. It is expected that reduction of the size of the oxidized lasers will lead to a linear decrease of the switching and holding currents and of the input light, which is an important consideration for closed packaged two-dimensional arrays of such devices.



(a)



(b)



(c)

Fig. 4. (a). Illustration of latchable optical switching using short optical pulses that impinge on the switch in the presence of a bias voltage pulse that exceeds the threshold of the VCL-DOT. Demonstration of digital optical logic operations (b). OR and (c). AND using a VCL-DOT. Each photograph contains four traces showing the bias voltage, optical inputs A and B, and the optical output pulses, respectively.

The latching optical switching characteristics of the optical thyristor under pulsed excitation are presented in Fig. 4(a). The bias is a periodic rectangular signal of  $6 \mu\text{s}$  width,  $10 \mu\text{s}$  duration, and amplitude with  $4.9 \text{ V}$ . Because the pulse voltage of  $4.9 \text{ V}$  is above the holding voltage, but is below the switching voltage in the dark, as shown in Fig. 3, it does not turn-on until an optical pulse of shorter duration impinges upon the VCL-DOT via an optical fiber. The optical pulse reduces the switching voltage below the  $4.9 \text{ V}$  bias, thus the operating

point moves to the high-conductance state. The VCL-DOT remains switched on after the optical pulse has subsided, and lasing persists until the switch is turned off electrically by switching off the bias. A small voltage drop is observed during the switch to the ON state, as the device is switched from a high-impedance state to a high-conductance state.

Figures 4(b) and 4(c) show experimentally the input-output oscilloscope traces of the optical switching characteristics of the AND and OR optical logic gates based on the VCL-DOT switch, respectively. Logic operations have been realized by connecting serial (AND gate) or parallel (OR gate) combinations of discrete optical thyristor switches [13, 14]. In this scheme, discrete input and output sites and multiple optical inputs deteriorate the integrability, induce thermal management problems. Here we demonstrate AND and OR logic using a monolithically integrated device. Two synchronously modulated optical (laser) sources are also used by our fabricated devices, because our fabricated device has multiple functions such as optical logic gates, optical switches, and optical sources. These two optical sources of 67 ns pulse width are guided by optical fibers to impinge upon a depleted optical thyristor input, while the vertical cavity laser output is collected by a Si photodetector using an optical coupler and splitter. The bias signal for the OR function has a signal duration of 133 ns and an amplitude of 5.20  $V_{p,p}$ . Figure 4(b) demonstrates the operation of the logical OR gate. However, if the amplitude of the bias signal is adjusted to 5.05  $V_{p,p}$  without changing other conditions, it allows the VCL-DOT to get the logical AND function as shown in Fig. 4(c). It is because one optical input signal does not have enough power to move the operating point from the off-state to the on-state; a driving voltage of 5.20  $V_{p,p}$  allows the operating point to move to the on-state even though only one optical signal is injected into the VCL-DOT. Consequently, the VCL-DOT using our scheme can be demonstrated as the optical logic AND- as well as OR-gate without complex electrical circuits.

#### 4. Conclusions

Latchable optical switches and logic gates are realized by the monolithic integration of a VCL-DOT grown on n-type substrate fabricated by selective oxidation. The PnpN optical thyristors clearly show a nonlinear s-shaped current-voltage and lasing characteristics. Digital AND and OR optical logic gates operation is experimentally demonstrated using our operating technique. The switching speed can be significantly improved by device scaling, optimization of the DOT structure's design, and selection of the optimal bias conditions. Our experimental results suggest the potential applications of VCL-DOT in advanced optical communication systems. For a practical use of the DOT in a free space optical interconnect further improvements are required in optical sensitivity and emission efficiency.

#### Acknowledgment

This work was partially supported by 'ERC OPERA (R11-2003-002)' and 'grant No. (R01-2005-000-10176-0) from the Basic Research Program of the Korea Science & Engineering Foundation'.